WHAT IS CLAIMED IS:

1. A liquid crystal display, comprising:

a first insulating substrate;

a black matrix formed on said first substrate, said black matrix being mesh-shaped with opening portions at pixel areas;

an insulating layer formed on and covering both said first substrate and said black matrix;

a gate line assembly formed on said insulating layer, said gate line assembly comprising gate lines proceeding in a horizontal direction, and gate electrodes connected to the gate lines;

a gate insulating pattern formed on and covering both said insulating layer and said gate line assembly;

a semiconductor pattern formed on said gate insulating pattern;

an ohmic contact layer formed on said semiconductor pattern;

a data line assembly formed on said ohmic contact layer, said data line assembly comprising a source electrode and a drain electrode separated from each other, and data lines connected to the source electrode while crossing over the gate lines to define the pixel areas; and

a protective layer covering said data line assembly and said gate line assembly while exposing said gate insulating pattern, said semiconductor pattern, and portions of said insulating layer placed at the pixel areas.

2. The liquid crystal display of claim 1, further comprising a pixel electrode connected to the drain electrode, said protective layer having a first contact hole

exposing the drain electrode, the connection of the pixel electrode to the drain electrode being made through the first contact hole.

3. The liquid crystal display of claim 2, wherein the black matrix is separated into plural numbers of portions.

4. The liquid crystal display of claim 2, further comprising buffer layers placed at the same plane as said gate line assembly or said data line assembly, the buffer layers being positioned between the neighboring separate portions of the black matrix.

5. The liquid crystal display of claim 2, wherein said black matrix comprises first portions overlapped with the gate lines, and second portions overlapped with the data lines, the first portions and the second portions of said black matrix being separated from each other.

6. The liquid crystal display of claim 2, wherein each pixel electrode has a peripheral portion overlapping said black matrix.

7. The liquid crystal display of claim 2, wherein said protective layer is formed in the same shape as said gate insulting pattern and the semiconductor pattern except the first contact holes.

8. The liquid crystal display of claim 2, wherein the borderlines of said protective layer, said gate insulating pattern, and said semiconductor pattern are placed over said black matrix except the area where the drain electrode is located.

9. The liquid crystal display of claim 2, further comprising:

gate pads connected to the gate lines to receive scanning signals from outside and transmitting the scanning signals to the gate lines, said gate insultaing pattern, said

semiconductor pattern and said protective layer having second contact holes exposing said gate pads;

data pads connected to the data lines to receive picture signals from outside and transmitting the picture signals to the data lines, said protective layer having a third contact holes exposing said data pads; and

subsidiary gate pads formed at the same plane as the pixel electrodes and connected to said gate pads through the second contact holes; and

subsidiary data pads formed at the same plane as the pixel electrodes and connected to said gate pads through the third contact holes.

10. The liquid crystal display of claim 9, wherein the protective layer is formed in the same shape as said gate insulating pattern and said semiconductor pattern except the first contact holes and the third contact holes.

11. The liquid crystal display of claim 2, further comprising buffer conductive layers positioned over said semiconductor pattern between the neighboring data lines, the buffer conductive layers being placed at the same plane as the pixel electrodes.

12. The liquid crystal display of claim 11, wherein the buffer conductive layers are connected to said gate line assembly.

13. The liquid crystal display of claim 2, further comprising:

buffer conductive layers positioned over the semiconductor pattern between the neighboring data lines while being placed at the same plane as said data line assembly, said protective layer having second contact holes exposing the gate lines and said buffer conductive layers; and

a connection pattern formed at the same plane as the pixel electrodes, said connection pattern connecting the gate lines to said buffer conductive layers through the second contact holes.

14. The liquid crystal display of claim 2, further comprising:

a second insulating substrate facing said first insulating substrate; and

a common electrode formed on said second insulating substrate, the common electrode having opening portions over said semiconductor pattern between the neighboring data lines.

15. A method for fabricating a thin film transistor substrate for a liquid crystal display, comprising the steps of:

forming a black matrix on an insulating substrate such that the black matrix is mesh-shaped with opening portions at pixel areas;

forming an insulating layer on the substrate such that the insulating layer covers the black matrix;

forming a gate line assembly on the insulating layer, the gate line assembly comprising gate lines proceeding in a horizontal direction, and gate electrodes connected to the gate lines;

depositing a gate insulating layer onto the insulating layer;

depositing a semiconductor layer onto the gate insulating layer;

forming an ohmic contact layer on the semiconductor layer;

forming a data line assembly on the ohmic contact layer, the data line assembly comprising a source electrode and a drain electrode separated from each other, and data lines connected to the source electrode while crossing over the gate lines to define

the pixel areas;

depositing a protective layer onto the substrate such that the protective layer covers the data line assembly and the gate line assembly; and

forming opening portions exposing the insulating layer at the pixel areas through patterning the protective layer, the gate insulating layer and the semiconductor layer.

16. The method of claim 15, further comprising the step of forming pixel electrodes such that the pixel electrodes are connected to the drain electrodes, first contact holes exposing the drain electrodes being formed at the protective layer at the step of forming the opening portions and the pixel electrodes connected to the drain electrodes through the first contact holes.

17. The method of claim 16, wherein the black matrix are separated into a number of portions.

18. The method of claim 16, wherein buffer layers are formed between the separate portions of the black matrix at the step of forming the gate line assembly or the data line assembly.

19. The method of claim 16, wherein each pixel electrode has a pheripheral portion overlapping with the black matrix.

20. The method of claim 16, wherein the protective layer is formed in the same shape as the gate insulating pattern and the semiconductor pattern except for the first contact holes.

21. The method of claim 16, wherein the borderlines of the protective layer, the gate insulating pattern and the semiconductor pattern are placed over the black

matrix except the area where the drain electrode is located.

22. The method of claim 16, further comprising the step of:

forming subsidiary gate pads and subsidiary data pads at the same plane as the pixel electrodes,

wherein the gate pads are formed at the step of forming the gate line assembly such that the gate pads are connected to the gate lines to receive scanning signals from outside and transmit the scanning signals to the gate lines, and the gate insultaing pattern, the semiconductor pattern and the protective layer have second contact holes exposing the gate pads,

wherein the data pads are formed at the step of forming the data line assembly such that the data pads are connected to the data lines to receive picture signals from the outside and transmit the picture signals to the data lines, and the protective layer has third contact holes exposing the data pads,

wherein the subsidiary gate pads are connected to the gate pads through the second contact holes, and

wherein the subsidiary data pads are connected to the data pads through the third contact holes.

23. The method of claim 22, wherein the protective layer is formed in the same shape as the gate insulating pattern and the semiconductor pattern except for the first contact holes and the third contact holes.

24. The method of claim 16, further comprising the step of forming buffer conductive layers such that the buffer conductive layers are positioned over the semiconductor pattern between the neighboring data lines, the buffer conductive layers

being placed at the same plane as the pixel electrodes.

25. The method of claim 16, further comprising the steps of:

forming buffer conductive layers such that the buffer conductive layers are positioned over the semiconductor pattern between the neighboring data lines while being placed at the same plane as the data line assembly, the protective layer having second contact holes exposing the gate lines and the buffer conductive layers; and

forming a connection pattern such that the connection pattern is placed at the same plane as the pixel electrodes, the connection pattern connecting the gate lines to the buffer conductive layers through the second contact holes.